CLAIMS

1. A method, comprising:

loading X bits at a time into a shift register and shifting groups of older, loaded X bits up in said shift register with each new group of loaded X bits, each group of X bits having been received from a serial data stream;

identifying an alignment key within said shift register; and,

presenting aligned data from said serial data stream by rotating selection of a first group of Y contiguous bits from said shift register and a second group of Y contiguous bits from said shift register after said identifying, Y being greater than X.

2. The method of claim 1 wherein said rotating further comprises selecting said first and second groups of Y contiguous bits with a multiplexer.

3. The method of claim 2 wherein said selecting further comprises providing to said multiplexer's channel select input, in a rotated fashion, the identity of said group of Y contiguous bits and the identity of said group of Y contiguous bits.

4. The method of claim 1 wherein said rotating is asymmetrical in that a first time period following selection of said second group of Y contiguous bits up to selection of said first group of Y contiguous bits is different than a second time period following selection of said first group of Y contiguous bits up to selection of said second group of Y contiguous bits.

5. The method of claim 1 wherein said shifter register is sized to hold Z bits where:

$Z = Xl + ((X/2)-1)$

and where:

(i) k = the rounded down integer of Y/X; and,

(ii) $l = k + 1$.

6. The method of claim 1 further comprising loading a value into a counter for said counter to start from, said value based upon where said alignment key is found within said shift register.

7. The method of claim 6 further comprising triggering the timing of said selection of said first group of Y contiguous bits upon said counter reaching a first value and triggering the timing of said selection of said second group of Y contiguous bits upon said counter reaching a second value.

8. The method of claim 7 wherein said first group of Y contiguous bits is the first group of Y bits to follow said alignment key in said serial data stream and said second group of Y contiguous bits is the second group of Y bits to follow said first group in said serial data stream.

9. An apparatus, comprising:

a parallel load shift register to receive a new input word of X bits;

X comparators, each comparator coupled to receive a different set of one or more contiguous bits of said new input word of X bits, each comparator to identify an alignment key located within said shift register;

a plurality of channels, each channel encompassing a different selection of Y contiguous bits within said shift register, each channel flowing to a different input of a multiplexer, Y being greater than X; and,

a control circuit coupled to an output from each of said comparators, said control circuit comprising a second multiplexer whose output is coupled to a channel select input of said multiplexer, said second multiplexer having a first input to identify a first of said channels and a second input to identify a second of said channels, said control circuit comprising a counter whose output is coupled to comparison logic, said comparison logic coupled to a channel select input of said second multiplexer to control the timing of when said first channel is selected by said multiplexer and when said second channel is selected by said multiplexer.

10. The apparatus of claim 9 further comprising a latch whose input is coupled to said multiplexer's output.

11. The apparatus of claim 10 wherein said comparison logic is coupled to said latch's clocking input so as to cause said latch to latch the content of said multiplexer's output when said first channel is selected by said multiplexer and when said second channel is selected by said multiplexer.

12. The apparatus of claim 9 wherein said counter has an input to receive a value where said counter should start counting from, said counter input coupled to an output of a third multiplexer, said third multiplexer having a first input to provide a first value where said counter should start counting from, said multiplexer having a second input to receive a second value where said counter should start counting from.

13. The apparatus of claim 12 where said third counter has a channel select input coupled to receive an indication whether a remaining portion of said alignment key resides within a first half of said new input word of X bits or a second half of said new input word of X bits, said first value to be provided to said counter if said remaining portion of said alignment key resides within said first half, said second value to be provided to said counter if said remaining portion of said alignment key resides within said second half.

14. The apparatus of claim 9 wherein said first input is coupled to a circuit that identifies where said alignment key has been found in said shift register.

15. The apparatus of claim 14 wherein said circuit comprises a latch and is coupled to an output from each of said comparators.

16. The apparatus of claim 15 further comprising logic circuitry that performs a roll by X/2 function, said logic circuitry having an input coupled to said circuit and an output coupled to said second input.

17. The apparatus of claim 9 wherein said shifter register is sized to hold Z bits where:

$Z = Xl + ((X/2)-1)$

and where:

(i) k = the rounded down integer of Y/X; and,

(ii) $l = k + 1$.

18. An apparatus, comprising:

a) a connector to receive an optical fiber;

b) a serial to parallel converter having an input coupled to said connector and an output that provides X bits at a time from said optical fiber; and,

c) an alignment key synchronization circuit, comprising:

(i) a parallel load shift register to receive a new input word of X bits from said serial to parallel converter;

(ii) X comparators, each comparator coupled to receive a different set of one or more contiguous bits of said new input word of X bits, each comparator to identify an alignment key located within said shift register;

(iii) a plurality of channels, each channel encompassing a different selection of Y contiguous bits within said shift register, each channel flowing to a different input of a multiplexer, Y being greater than X;

(iv) a control circuit coupled to an output from each of said comparators, said control circuit comprising a second multiplexer whose output is coupled to a channel select input of said multiplexer, said second multiplexer having a first input to identify a first of said channels and a second input to identify a second of said channels, said control circuit comprising a counter whose output is coupled to comparison logic, said comparison logic coupled to a

channel select input of said second multiplexer to control the timing of when said first channel is selected by said multiplexer and when said second channel is selected by said multiplexer.

19. The apparatus of claim 18 further comprising a latch whose input is coupled to said multiplexer's output.

20. The apparatus of claim 19 wherein said comparison logic is coupled to said latch's clocking input so as to cause said latch to latch the content of said multiplexer's output when said first channel is selected by said multiplexer and when said second channel is selected by said multiplexer.

21. The apparatus of claim 18 wherein said counter has an input to receive a value where said counter should start counting from, said counter input coupled to an output of a third multiplexer, said third multiplexer having a first input to provide a first value where said counter should start counting from, said multiplexer having a second input to receive a second value where said counter should start counting from.

22. The apparatus of claim 21 where said third counter has a channel select input coupled to receive an indication whether a remaining portion of said alignment key resides within a first half of said new input word of X bits or a second half of said new input word of X bits, said first value to be provided to said counter if said remaining portion of said alignment key resides within said first half, said second value to be provided to said counter if said remaining portion of said alignment key resides within said second half.

23. The apparatus of claim 18 wherein said first input is coupled to a circuit that identifies where said alignment key has been found in said shift register.

24. The apparatus of claim 23 wherein said circuit comprises a latch and is coupled to an output from each of said comparators.

25. The apparatus of claim 24 further comprising logic circuitry that performs a roll by X/2 function, said logic circuitry having an input coupled to said circuit and an output coupled to said second input.

26. The apparatus of claim 18 wherein said shifter register is sized to hold Z bits where:

$Z = Xl + ((X/2)-1)$

and where:

(i) k = the rounded down integer of Y/X; and,

(ii) l = k + 1.